2.7 V to 5.25 V, Micro Power, Dual-Channel, 200 kSPS, 12-Bit ADC in 8-Pin µSOIC

Preliminary Technical Data — AD7887

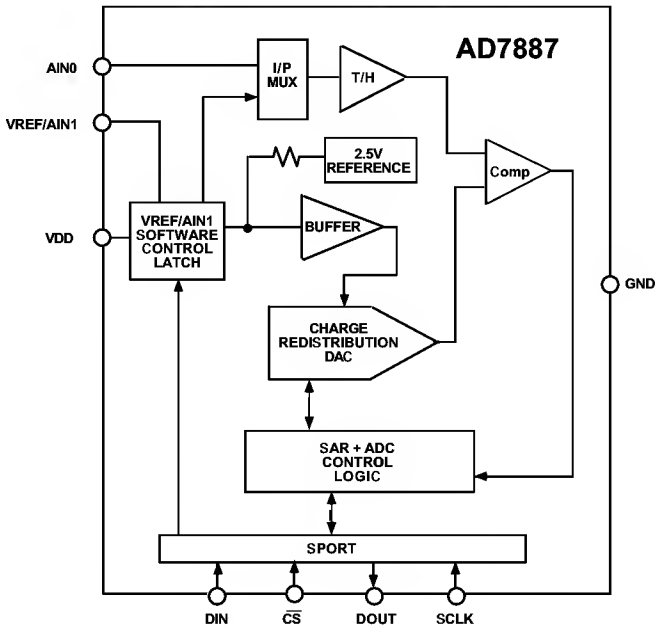
FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V
200ksps at 5V Supplies
125ksps at 3V Supplies
Flexible Power/Throughput Rate Management
700 µA max @ 200 kSPS Throughput.
70 µA max @ 10 kSPS Throughput
Shut Down Mode: 1µA max
One/Two Single-Ended Inputs
Serial Interface: SPI/QSPI/µWire/DSP
8-Pin Narrow SOIC and µSOIC Packages

APPLICATIONS

Battery-Powered Systems (Personal Digital Assistants, Medical Instruments, Mobile Communications)
Instrumentation and Control Systems
High Speed Modems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7887 is a high speed, low power, 12-bit ADC that operates from a single 2.7 V to 5.25 V power supply. The AD7887 is capable of 200 ksps throughput rate. The input track-and-hold acquires a signal in 500 ns and features a single ended sampling scheme. The output coding for the AD7887 is straight binary and the part is capable of converting full power signals up to 3MHz.

The AD7887 can be configured for either dual or single channel operation, via the on-chip Control Register.There is a default single-channel mode which allows the AD7887 to be operated as a read-only ADC. In single-channel operation, there is one analog input (AIN0) with the V_{REF}/AIN1 pin assuming its V_{REF} function. This V_{REF} pin allows the user access to the part's internal +2.5V reference or the V_{REF} pin can be overdriven by an external reference to provide the reference voltage for the part. This external reference volatge has a range of +2.5V to V_{DD}. The analog input range on AIN0 is 0 to +V_{REF}.

In dual-channel operation, the V_{REF}/AIN1 pin assumes its AIN1function, providing a second analog input channel. In this case, the reference volatge for the part is provided via the V_{DD} pin. As a result, the input voltage range on both the AIN0 and AIN1 inputs is 0 to V_{DD}.

CMOS construction ensures low power dissipation of typically 2 mW for normal operation and 3 µW in power-down mode. The part is available in a 8 -lead narrow body small outline (SOIC) and a 8 -lead micro small outline (µSOIC) package.

PRODUCT HIGHLIGHTS

1. Smallest 12-Bit Dual/Single -Channel ADC; 8 -lead micro small outline (µSOIC) package.
2. Lowest Power 12-Bit Dual/Single-channel ADC.
3. Flexible power management options including automatic powerdown after conversion.
4. Read-Only ADC Capability.
5. Analog input range from 0 V to V_{REF}.
6. Versatile serial I/O port (SPI/QSPI/µWire/DSP Compatible).

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AD7887–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, V_{REF} = 2.5 V External/Internal Reference unless otherwise noted, f_{SCLK} = 3.2 MHz (VDD=+4.75V to +5.25V); f_{SCLK} = 2 MHz (VDD=+2.7V to +3.6V); T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE				
Signal to Noise + Distortion Ratio[2] (SNR)	70	71	dB min	Typically SNR is 72 dB V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz
Total Harmonic Distortion (THD)	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz
Peak Harmonic or Spurious Noise	–78	–78	dB max	V_{IN} = 10 kHz Sine Wave, f_{SAMPLE} = 200 kHz
Intermodulation Distortion (IMD)				
Second Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz
Third Order Terms	–78	–80	dB typ	fa = 9.983 kHz, fb = 10.05 kHz, f_{SAMPLE} = 200 kHz
Channel-to-Channel Isolation	–90	–90	dB typ	V_{IN} = 25 kHz
Full Power Bandwidth			MHz typ	@ 3 dB
DC ACCURACY				Any Channel
Resolution	12	12	Bits	
Integral Nonlinearity	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed No Missed Codes to 12 Bits.
Total Unadjusted Error	±3	±3	LSB typ	
Offset Error	±3	±3	LSB max	
Offset Error Match	3	3	LSB max	
Positive Full-Scale Error	±3	±3	LSB max	
Positive Full-Scale Error Match	3	3	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to V_{REF}	0 to V_{REF}	Volts	
Leakage Current	±1	±1	µA max	
Input Capacitance	20	20	pF typ	
REFERENCE INPUT/OUTPUT				
REF_{IN} Input Voltage Range	2.3/V_{DD}	2.3/V_{DD}	V min/max	Functional from 1.2 V
Input Impedance	10	10	kΩ typ	
REF_{OUT} Output Voltage	2.4/2.6	2.4/2.6	V min/max	
REF_{OUT} Tempco	20	20	ppm/°C typ	
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	V_{DD} = 4.75 V to 5.25 V
	2.1	2.1	V min	V_{DD} =2.7 V to 3.6V
Input Low Voltage, V_{INL}	0.8	0.8	V max	V_{DD} = 2.7 V to 5.25 V
Input Current, I_{IN}	±10	±10	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}				I_{SOURCE} = 200 µA
	V_{DD} -0.5	V_{DD} -0.5	V min	V_{DD} = 2.7 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} =200µA
Floating-State Leakage Current	±10	±10	µA max	
Floating-State Output Capacitance[4]	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Throughput Time	16	16	SCLK cycles	Conversion Time + Acquisition Time. 200ksps with 3.2MHz clock and 125ksps with 2MHz clock
Track/Hold Acquisition Time	1.5	1.5	SCLK cycles	
Conversion Time	14.5	14.5	SCLK cycles	4.5µs (3.2MHz clock); 7.25µs (2MHz clock)

Parameter	A Version[1]	B Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25	+2.7/+5.25	V min/max	
I_{DD}				
Normal Mode[4]	700	700	μA max	
Using Standby Mode	450	450	μA max	f_{SAMPLE} = 100 ksps
Using Shutdown Mode	70	70	μA max	f_{SAMPLE} = 10 ksps
Using Shutdown Mode	8	8	μA max	f_{SAMPLE} = 1 ksps
Standby Mode	200	200	μA max	V_{DD} = 2.7 V to 5.25 V
Shutdown Mode	3	3	μA max	V_{DD} = 4.75 V to 5.25 V
Shutdown Mode	1	1	μA max	V_{DD} = 2.7 V to 3.6 V
Normal Mode Power Dissipation	3.5	3.5	mW max	V_{DD} = 5V.
	2.1	2.1	mW max	V_{DD} = 3V
Shutdown Power Dissipation	15	15	μW max	V_{DD} = 5 V
	3	3	μW max	V_{DD} = 3 V
Standby Power Dissipation	1	1	mW max	V_{DD} = 5V
	600	600	μW max	V_{DD} = 3V

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3]Sample tested @ +25°C to ensure compliance.
[4]All digital inputs @ GND except $\overline{CS}$ @ V_{DD}. No load on the digital outputs. Analog inputs @ GND.
[5]SCLK @ GND when SCLK off. All digital inputs @ GND except for $\overline{CS}$ @ V_{DD}. No load on the digital outputs. Analog inputs @ GND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND ..... –0.3 V to +7 V
V_{DD} to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND ..... –0.3 V to V_{DD} + 0.3 V
REF_{IN}/REF_{OUT} to AGND ..... –0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range
Commercial (A, B Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
μSOIC, SOIC Package, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance .. 140°C/W (μSOIC) 160°C/W (SOIC)
θ_{JC} Thermal Impedance .. 44°C/W (μSOIC) 56°C/W (TSSOP)
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infared (15 secs) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Linearity Error (LSB)[1]	Package Option[2]
AD7887AR	±2	R-8
AD7887BR	±1	R-8
AD7887ARM	±2	RM-8
EVAL-AD7887CB[3]	Evaluation Board	
EVAL-CONTROL BOARD[4]	Controller Board	

NOTES
[1]Linearity error here refers to integral linearity error.
[2]R = SOIC; RM = μSOIC.
[3]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[4]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS[1]

Parameter	Limit at T_{MIN}, T_{MAX} (A, B Versions) 4.75 to 5.25 V	2.7 to 3.6V	Units	Description
f_{SCLK}	3.2	3.2	MHz max	V_{DD} = +4.75V to +5.25 V
	2	2	MHz max	V_{DD} = +2.7 V to +3.6 V
$t_{CONVERT}$	14.5 t_{SCLK}	14.5 t_{SCLK}		Throughput Time = $t_{CONVERT}$ + t_{acq} = 16 t_{SCLK}
t_{acq}	1.5 t_{SCLK}	1.5 t_{SCLK}		Throughput Time = $t_{CONVERT}$ + t_{acq} = 16 t_{SCLK}
t_1	tbd	tbd	ns min	$\overline{CS}$ to SCLK Setup Time
t_2[3]	50	90	ns max	Delay from $\overline{CS}$ Until DOUT 3-State Disabled
t_3[3]	0	0	ns min	DIN Time Following $\overline{CS}$
t_4[3]	75	115	ns max	Data Access Time After SCLK Falling Edge
t_5	40	60	ns min	Data Setup Time Prior to SCLK Rising Edge
t_6	20	30	ns min	Data Valid to SCLK Hold Time
t_7	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK High Pulse Width
t_8	0.4 t_{SCLK}	0.4 t_{SCLK}	ns min	SCLK Low Pulse Width
t_9	tbd	tbd	ns min	SCLK to $\overline{CS}$ Hold Time
t_{10}[4]	50	50	ns max	$\overline{CS}$ Rising Edge to DOUTHigh Impedance

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts.

[2]Mark/Space ratio for the SCLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_{10} is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_{10}, quoted in the timing characteristics is thetrue bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

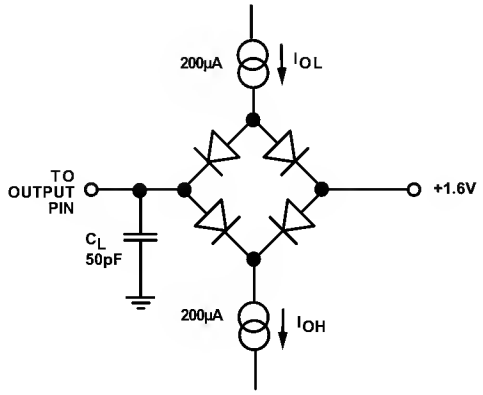
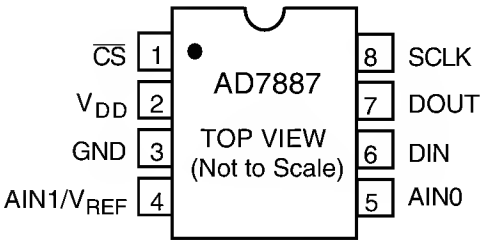


Figure 1. Load Circuit for Digital Output Timing Specifications

PIN CONFIGURATION



PIN FUNCTION DESCRIPTION

Pin No.	Pin Mnemonic	Function
1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7887 and also frames the serial data transfer.When the AD7887 operates in its default mode, the $\overline{CS}$ pin also acts as the shutdown pin such that with the $\overline{CS}$ pin high, the AD7887 is in its power-down mode.
2	V_{DD}	Power Supply Input. The V_{DD} range for the AD7887 is from +2.7V to +5.25V. When the AD7887 is configured for two-channel operation, this pin also provides the reference source for the part.
3	GND	Ground pin. This pin is the ground reference point for all circuitry on the AD7887. In systems with separate AGND and DGND planes, these planes should be tied together as close as possible to this GND pin. Where this is not possible, this GND pin should connect to the AGND plane.
4	AIN1/V_{REF}	Analog Input 1/Voltage Reference Input. In single-channel mode, this pin becomes the refernce input/ouput. In this case, the user can either access the internal +2.5V reference or overdrive the internal reference with the voltage applied to this pin. The reference voltage range for an externally-applied refernce is 1.2V to V_{DD}. In two-channel mode, this pin provides the second analog input channel AIN1. The input volatge range on AIN1 is 0 to V_{DD}.
5	AIN0	Analog Input 0. In single-channel mode, this is the analog input and the input volatage range is 0 to V_{REF}. In dual-channel mode, it has an analog input range of 0 to V_{DD}.
6	DIN	Data In. Logic Input. Data to be written to the AD7887's Control Register is provided on this input and is clocked into the register on the falling edge of SCLK (see Control Register section). The AD7887 can be operated as a single-channel read-only ADC by tying the DIN line permanently to GND.
7	DOUT	Data Out. Logic Output.The conversion result from the AD7887 is provided on this output as a serial data stream. The bits are clocked out on the rising edge of the SCLK input. The data stream consists of four leading zeros followed by the 12-bits of conversion data which is provided MSB first.
8	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part and writing serial data to the Control Register. This clock input is also used as the clock source for the AD7887's conversion process.

CONTROL REGISTER

The Control Register on the AD7887 is an 8-bit, write-only register. Data is loaded from the DIN pin of the AD7887 on the falling edge of SCLK. The data is transferred on the DIN line at the same time as the conversion result is read from the part. This requires 16 serial clocks for every data transfer. Only the information provided on the first 8 falling clock edges (after $\overline{CS}$) is loaded to the Control Register. MSB denotes the first bit in the data stream. The bit functions are outlined in Table I.

Table I. Control Register

MSB

DONTC	ZERO	REF	SIN/DUAL	CH	ZERO	PM1	PM0

DONTC — Don't Care. The value written to this bit of the Control Register is a don't care i.e. it doesn't matter if the bit is 0 or 1.

ZERO — A zero must be written to this bit to ensure correct operation of the AD7887.

REF — Reference bit. With a 0 in this bit, the on-chip reference is enabled. With a 1 in this bit, the on-chip reference is disabled.

SIN/DUAL — Single/Dual Bit. This bit determines whether the AD7887 operates in single-channel or dual-channel mode. A 0 in this bit selects single-channel and the AIN1/V_{REF} pin assumes its V_{REF} function. A 1 in this bit selects dual-channel mode and the reference voltage for the ADC is internally connected to V_{DD} and the AIN1/V_{REF} pin assumes it AIN1 function as the second analog input channel.

CH — Channel Bit. When the part is selected for dual-channel mode, this bit determines which channel will be converted for the next conversion. A 0 in this bit selects the AIN0 input while a 1 in this bit selects the AIN1 input. In single-channel mode, this bit should always be 0.

ZERO — A zero must be written to this bit to ensure correct operation of the AD7887.

PM1, PM0 — Power Management Bits. This two bits decode the mode of operation of the AD7887 as described below.

PM1	PM0	Mode
0	0	Mode 1. In this mode, the AD7887 enters shutdown if the $\overline{CS}$ input is 1 and is in full power mode when $\overline{CS}$ is 0. Thus the part comes out of shutdown on the falling edge of $\overline{CS}$ and enters shutdown on the rising edge of $\overline{CS}$.
0	1	Mode 2. In this mode, the AD7887 is always fully powered-up regardless of the status of any of the logic inputs.
1	0	Mode 3. In this mode, the AD7887 automatically enters shutdown mode at the end of each conversion regardless of the state of $\overline{CS}$.
1	1	Mode 4. In this standby mode where portions of the AD7887 are powered down but the on-chip reference voltage remains powered-up. It means that the reference volatge is available for use external to the AD7887 when in Standby. The REF bit should be 0 to ensure the on-chip reference is enabled.

CIRCUIT INFORMATION

The AD7887 is a fast, low-power, 12-bit, single supply, single-channel/dual-channel A/D converter. The part can be operated from +3V (+2.7V to +3.6V) supply or from +5V (+4.75V to +5.25V) supply. When operated from a +5V supply, the AD7887 is capable of throughput rates of 200ksps when provided with a 3.2MHz clock. When operated from +3V supplies, the clock is restricted to 2MHz allowing a throughput rate of 125ksps.

The AD7887 provides the user with an on-chip track/hold, A/D converter, reference and serial interface housed in an 8-pin package. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The part can be configured for single-channel or dual-channel operation. When configured as a single-channel part, the analog input range is 0 to V_{REF} (where the externally-applied VREF can be between +1.2V and V_{DD}). When the AD7887 is configured for two input channels, the input range is determined by internal connections to be 0 to VDD.

If single-channel operation is required, the AD7887 can be operated in a read-only mode by tying the DIN line permanently to GND. For applications where the user wants to change the mode of operation or wants to operate the AD7887 as a dual-channel A/D converter, the DIN line can be used to clock data into the part's Control Register.

MODES OF OPERATION

The AD7887 has a number of different modes of operation. These are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements. The modes of operation are controlled by the PM1 and PM0 bits of the Control Register as outlined previously. For read-only operation of the AD7887, the default mode of all 0's in the Control Register can be set up by tying the DIN line permanently low.

Mode 1 (PM1=0, PM0=0)

This mode allows the user to control the powering-down of the part via the $\overline{CS}$ pin. Whenever $\overline{CS}$ is low, the AD7887 is in its fully-powered mode; whenever $\overline{CS}$ is high, the AD7887 is in its power-down mode. When $\overline{CS}$ goes from high to low, all on-chip circuitry starts to power up. It takes approximately, 5us for the AD7887 internal circuitry to be fully powered-up. As a result, a conversion (or sample-an-hold acquisition) should not be initiated during this 5us.

Figure 2 shows a general diagram of the operation of the AD7887 in this mode. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. The user should ensure that 5us elapses between the falling edge of $\overline{CS}$ and the first rising edge of SCLK. In microcontroller applications, this is readily achievable by driving the $\overline{CS}$ input from one of the port lines and ensuring that the serial data read (from the microcontrollers serial port) is not initiated for 5us. In DSP applications, where the $\overline{CS}$ is generally derived from the serial frame synchronisation line, it is usually not possible to separate the $\overline{CS}$ falling edge and SCLK by up to 5us. Therefore, the user will need to write to the Control Register to exit this mode and (by writing PM1=0 and PM0=1) put the part into Mode 2. A second conversion will then need to be initiated when the part is powered-up to get a conversion result. The write operation which takes place in conjunction with this second conversion can put the part back into Mode 1 and the part will go into power-down mode when $\overline{CS}$ returns high.

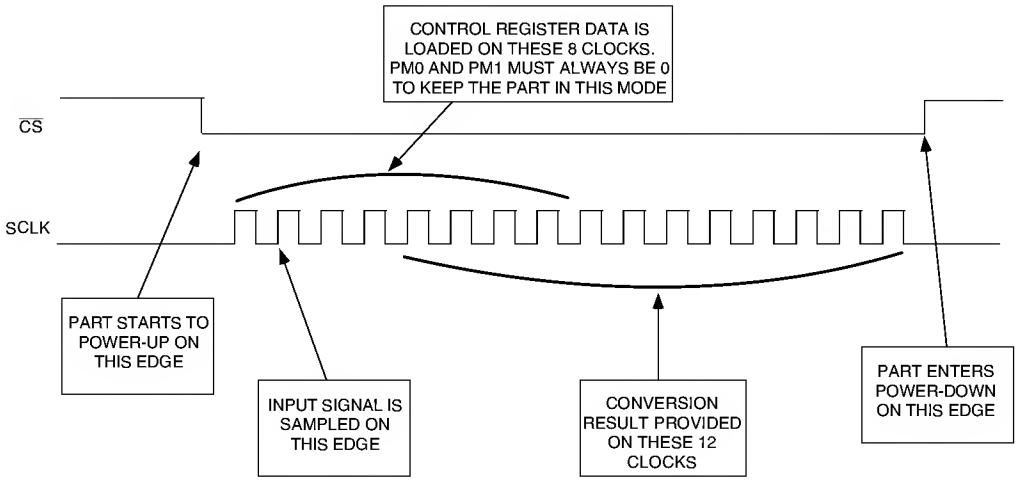


Figure 2. MODE 1 Operation

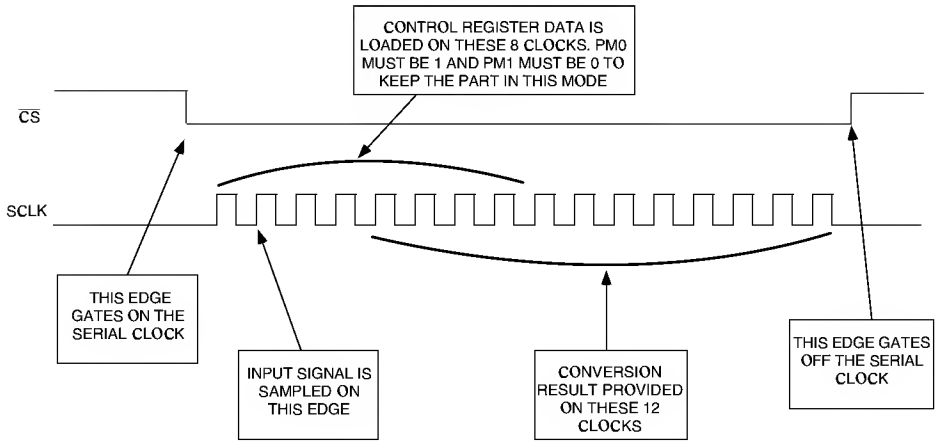


Figure 3. MODE 2 Operation

Mode 2 (PM1=0, PM0=1)
In this mode of operation, the AD7887 remains fully powered-up regardless of the status of the $\overline{CS}$ line. It is intended for fastest throughput rate performance as the user does not have to worry about the 5us power-up time mentioned previously. Figure 3 shows the general diagram of the operation of the AD7887 in this mode.

The data presented to the AD7887 on the DIN line during the first eight clock cycles of the data transfer are loaded to the Control Register. To continue to operate in this mode, the user must ensure that PM1 is loaded with 0 and PM0 is loaded with 1 on every data transfer.

The falling edge of $\overline{CS}$ initiates the sequence and the input signal is sampled on the second rising edge of the SCLK input. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. Once a data transfer is complete ($\overline{CS}$ has returned high), another conversion can be initiated immediately by bringing $\overline{CS}$ low again.

Mode 3 (PM1=1, PM0=0)
In this mode, the AD7887 automatically enters its power-down mode at the end of every conversion. It is similar to Mode 1 except that the status of $\overline{CS}$ does not have any effect on the power-down status of the AD7887.

Figure 4 shows the general diagram of the operation of the AD7887 in this mode. When $\overline{CS}$ goes from high to low, all on-chip circuitry starts to power up. It takes approximately, 5us for the AD7887 internal circuitry to be fully powered-up. As a result, a conversion (or sample-and-hold acquisition) should not be initiated during this 5us. The input signal is sampled on the second rising edge of SCLK following the $\overline{CS}$ falling edge. The user should ensure that 5us elapses between the falling edge of $\overline{CS}$ and the first rising edge of SCLK. In microcontroller applications, this is readily achievable by driving the $\overline{CS}$ input from one of the port lines and ensuring that the serial data read (from the microcontrollers serial port) is not initiated for 5us. In DSP applications, where the $\overline{CS}$ is generally derived from the serial frame synchronisation line, it is not possible to separate the $\overline{CS}$ falling edge and SCLK by up to 5us. Therefore, the user will need to write to the Control Register to exit this mode and (by writing PM1=0 and PM0=1) put the part into Mode 2. A second conversion will then need to be initiated when the part is powered-up to get a conversion result.The write operation which takes place in conjunction with this second conversion can put the part back into Mode 3 and the part will go into power-down mode when the conversion sequence ends.

Mode 4 (PM1=1, PM0=1)
In this standy mode, all on-chip circuitry, apart from the on-chip reference, is powered-down. The mode is useful for applications where the AD7887 is being powered-down but the on-chip reference is required for use external to the part.

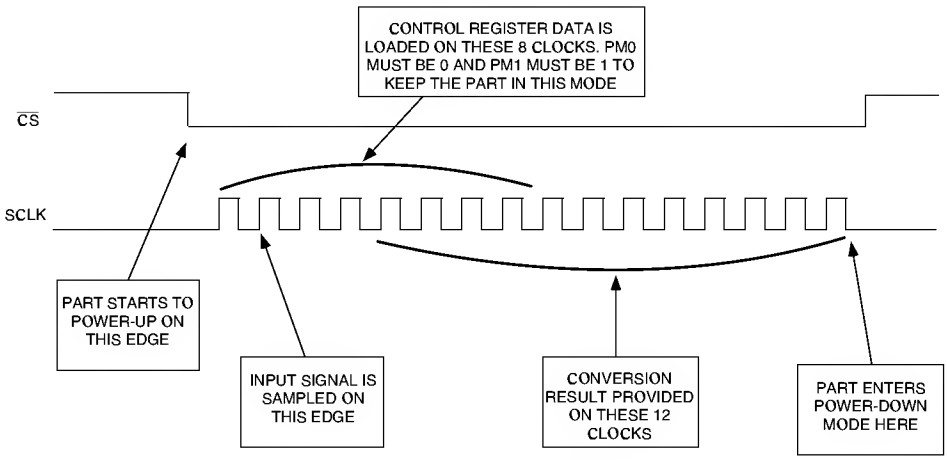


Figure 4. MODE 3 Operation

SERIAL INTERFACE

Figure 5 shows the detailed timing diagrams for serial interfacing to the AD7887. The serial clock provides the conversion clock and also controls the transfer of information to and from the AD7887 during conversion.

$\overline{CS}$ initiates the data transfer and conversion process. For some modes, the falling edge of $\overline{CS}$ wakes up the part. In all cases, it gates the serial clock to the AD7887 and puts the on-chip track/hold into track mode. The input signal is sampled on the second rising edge of the SCLK input after the falling edge of $\overline{CS}$. Thus, the first one and one-half clock cycles after the falling edge of $\overline{CS}$ are when the acquisition of the input signal takes place. This time is denoted as the acquisition time (t_{acq}). In modes where the falling edge of $\overline{CS}$ wakes up the part, the acquisition time must allow for the wake-up time of 5us. The on-chip track/hold goes from track mode to hold mode on the second rising edge of SCLK and a conversion is also initiated on this edge. The conversion process takes a further fourteen and one-half SCLK cycles to complete.

In dual-channel operation, the input channel which is sampled is the one which was selected in the previous write to the Control Register. Thus, in dual-channel operation the user must write ahead the channel for conversion. In other words, the user must write the channel address for the next conversion while the present conversion is in progress.

Writing of information to the Control Register takes place on the first 8 rising edges of SCLK in a data transfer. The Control Regsiter is always written to when a data transfer takes place. However, the AD7887 can be operated in a read-only mode by tying DIN low, thereby loading all 0's to the Control Register every time. When operating the AD7887 in write/read mode, the user must be careful to always set up the correct information on the DIN line when reading data from the part.

Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7887. Data is provided on the sixteen rising edges of SCLK in the conversion process. The first rising clock edge on the SCLK clock has the first leading zero provided. Subsequent bits are clocked out on the falling edge of SCLK so that they are provided to the processor on the following rising edge Thus, the second leading zero is clocked out on the falling edge subsequent to the first rising edge and the first bit of the conversion result (MSB) is provided on the fifth rising clock edge having been clocked out on the previous falling edge. The final bit in the data transfer is provided on the sixrteenth rising edge, having being clocked out on the previous falling edge.

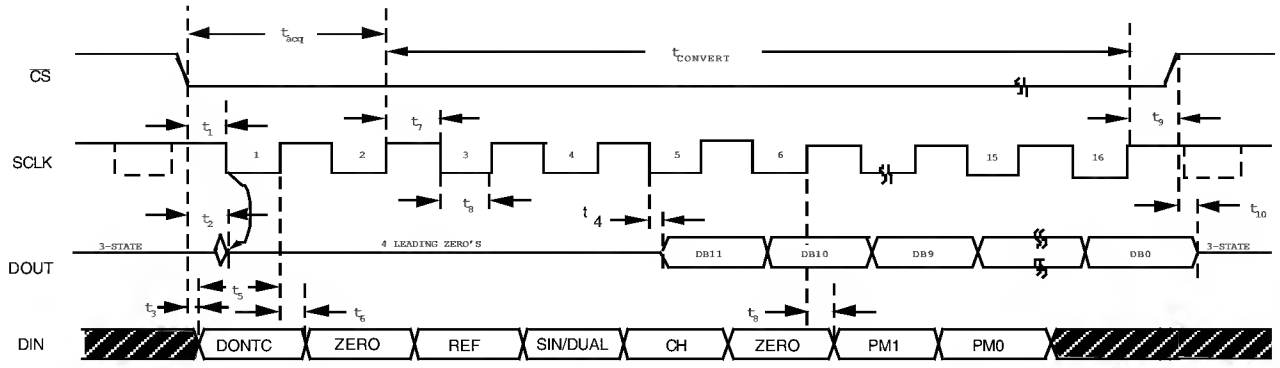


Figure 5. Serial Interface Timing Diagram